REPORT CTSL– 35

A 25 INPUT PULSE HEIGHT RECORDING SYSTEM

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JULY 11, 1962

SYNCHROTRON LABORATORY

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Supported in part by the U.S. Atomic Energy Commission
Contract No. AT(11-1)-68

Contents

Abstract

A general description is given of a data recording system which provides a link between counter experiments in high-energy physics and a high-speed digital computer. The instrument described can accept as many as 25 simultaneous photomultiplier tube signals and pulse height analyze them into 100 channels each. Six bits of digital data may be substituted for any unused pulse height input. The usual output is perforated paper tape with a binary coded decimal format for use with a Burroughs 220 computer. Identification words can be set up and recorded on the tape. The speed of the paper tape perforator limits the rate of analysis to one event per second. If the output data is fed directly into a computer memory, then the recording rate can be increased to 60 events per second. The instrument has been in operation since December 1961, and results obtained with it using both particles produced by the Caltech Synchrotron and pulsers are given. Only solid state components have been used, including nearly 1700 transistors and an equal number of diodes.

I. INTRODUCTION

In high-energy physics experiments it is sometimes desirable to record large quantities of correlated pulse height information in a form suitable for a digital computer. In the past, the pulses to be analyzed were often photographed on an oscilloscope, and the resulting film was manually analyzed. Because of the intrinsic low speed and limited precision and accuracy of this technique, we wished to automate the recording of the output of an experimental counter array presently being used with the Caltech Synchrotron. A pulse height recording system for this task has now been constructed in collaboration with Ransom Research, a Division of Wyle Laboratories, of San Pedro, California, and is commercially available under the name Model 1138B Sampling Digitizer (Fig. 1).

Earlier instruments have been described for the recording of correlated pulse height information from two or three simultaneous inputs. A system described by M. Birk et al.,[1] accepts two simultaneous inputs which are pulse height analyzed into 128 channels each. The results appear on punched paper tape which could be processed by a computer, although Birk et al., found this not to be necessary in their case. A system reported by C. C. Rockwood and M. G. Strauss[2] can pulse height or time analyze three simultaneous inputs into 256 channels each. The output of this system is magnetic tape, further processed manually with the aid of specialized equipment.

The instrument described here has 25 pulse height (Analog) inputs and is intended to provide paper tape for use with a digital computer. When the instrument is triggered by preselection circuits, a 5μs gate is

opened which allows pulses at the 25 Analog Inputs to be accepted, stored, and subsequently pulse height analyzed into 100 channels each, with an accuracy better than ± 0.5 per cent of full scale. These pulses may come from photomultiplier tubes directly or by way of fast gates, or they may be the output of other circuits, such as chronotrons. The output of the Sampling Digitizer appears in the form of paper tape punched in a binary coded decimal notation suitable for the input of the Burroughs 220 computer on the Caltech campus. We would have preferred the speed and compact data storage of magnetic tape, but the Burroughs 220 Magnetic Tape Unit is incapable of reliably reading externally written tape. The Sampling Digitizer has been designed so that conversion to magnetic tape for an IBM 7090 would not be too difficult.

Six Digital Inputs may be substituted for any unused Analog Input. During the 5μs input gate, the instrument records whether pulses on the selected Digital Inputs exceed a given level. These inputs can be used, for example, to record the outputs of coincidence circuits or scalers.

The high degree of complexity led to strong emphasis on a reliable design. Only solid-state components were used, with transistors being employed exclusively for the active elements. The digital control circuits were conservatively designed so that large variations in transistor parameters and pulse amplitudes could be tolerated. Also, in order to reduce the complexity, the analysis of the twenty-five Analog Inputs is performed serially, removing the need for twenty-five separate analog to digital converters. The instrument is provided with internal checking circuits and monitors so that proper operation can be easily ascertained.

II. GENERAL DESCRIPTION

A functional block diagram is shown in Fig. 2. We present here only a summary of the sequence of operations following a preselection trigger pulse. Because the Parallel to Serial Converter presented some unique problems in solid-state circuit design, it is discussed further in the next section. Details of the technique of analog to digital conversion used here are given in the Appendix.

The sequence of operations is determined by the Control. This section consists of digital logic circuits, whose operation is synchronized to a crystal controlled oscillator. Clock pulses derived from this oscillator are counted to generate all critical timing signals. Although the Control is rather complex, it contains only standard digital techniques, and its internal operation will not be discussed in further detail.

The overall operation of the instrument is controlled by a "Count Gate", which is either internally generated or controlled by an externally provided Beam Gate signal, which is ON during the period when the synchrotron is producing a photon beam. Only when the Count Gate is open can the Sampling Digitizer accept events consisting of input signals in coincidence with a trigger pulse. After the arrival of an accepted trigger pulse, the Input Gates at each Analog Input are opened for 5μs. Pulses which appear at the Analog Inputs during this period are accepted and stored by the Parallel to Serial Converter. The stored analog information is then presented at the output of this Converter as a sequence of twenty-five 320μs wide pulses whose amplitudes are proportional to the input pulse heights. These pulses are fed to the input of the Analog

to Digital Converter which generates a binary-coded two-digit decimal number for each successive input pulse. These numbers, together with the gated Digital Inputs, are recorded in a 200 binary bit Temporary Storage. The Parallel to Serial Converter is then reset in preparation for another trigger. The analysis and reset cycle described above requires about 16 ms when all 25 Analog Inputs are used.

Although the Temporary Storage and the Analog to Digital Converter have sufficient capacity for 256 pulse height channels (8 bits) per Analog Input, the restriction to the binary-coded decimal notation required by the Burroughs 220 limits the Sampling Digitizer to 100 pulse height channels. Similarly, only six of the eight Digital Inputs capable of being accepted by the Temporary Storage for each unused Analog Input can be used with binary-coded decimal notation.

Once an event has been recorded in the Temporary Storage, the closing of the Count Gate initiates the readout sequence, during which the Data Multiplexer scans the information in the Temporary Storage, the sign digits which are determined by preset front panel switches, and the end of word character, which is the number 13 generated by internal DC voltages. These are combined to produce standard Burroughs 220 Computer Words, which begin with a sign digit, then contain ten decimal digits from the Temporary Storage, and end with an end of word character. The output of the Data Multiplexer controls the operation of a paper tape perforator,* that is capable of operating at 72 characters per second. The capacity of the

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* The perforator which we are using was manufactured by the Tally Register Corporation of Seattle, Washington, and is a special modification of their Model 420PR.

Temporary Storage is five words, which require 845 ms to read out. If the entire capacity of the Temporary Storage is not used, time and paper tape may be saved by setting the readout to operate on only those words used. Since the synchrotron pulses each 1.05 seconds, about 200 ms are available during each pulse for collecting data. This is also the maximum time during which the synchrotron produces a photon beam.

In an alternative mode of operation concerned with events requiring less than 80 bits, more than one such event can be placed in the 200 bit Temporary Storage before read out. For example, when only ten Analog Inputs (or the equivalent number of Digital Inputs) are used, two events may be stored before read out. Similarly, if only five Analog Inputs are used, five events may be stored before read out. Since the analysis of such an event requires about 10 ms, but 845 ms are required to read out the Temporary Storage, this mode of operation reduces the instrument dead time at the expense of fewer inputs.

In a third mode of operation, the Data Multiplexer scans digits which have been set up on front panel switches rather than those in the Temporary Storage. These preset digits serve as identification words on the tape.

Usually, the signals entering the Analog Inputs have been obtained from the outputs of fast gates, which, ideally, should allow only one signal to pass through each Input Gate of the Sampling Digitizer during a single 5μs input gating pulse. The Fast Gate Inhibit circuit provides for inhibiting the 50 ns pulse that operates the fast-gating circuits.

Before a trigger is received, the Input Gate is closed, and fast-gating pulses are passed by the Fast Gate Inhibit circuit. After a trigger is accepted, the Input Gate will open in coincidence with the arrival at the Input Gate of the Analog Input signals, which have been delayed in the Sampling Digitizer by 1μs. The fast-gating pulses are then blocked by the Fast Gate Inhibit circuit during the 5μs duration of the input gating pulse. If the delay between the outputs of the fast gates and the Analog Inputs is negligible, then only during this 1μs period could more than one signal pass through an Input Gate. In addition, two types of slow (1/2 μs) pulses are derived from the fast-gating pulses. One of these appears for every fast-gating pulse entering the Fast Gate Inhibit circuit, and the other appears only when one of these fast-gating pulses has been blocked by the input gating pulse. These slow pulses are used to drive scalers for monitoring the number of fast-gating pulses generated and the number inhibited.

The number of analyzed events and the number of triggers passed by the Count Gate are counted by a decimal scaler. The difference of these counts is the number of events lost due to the system dead time.

Several provisions are made for testing various sections of the Sampling Digitizer. One test circuit reads arbitrary two-digit numbers into the Temporary Storage in order to test the Temporary Storage and its readout. The A/D Converter can be tested by applying either an internal or an external calibration voltage to its input. A two-decimal digit display indicates the pulse height of any Analog Input selected by a

front panel switch. A test pulser is provided which supplies a trigger and 25 simulated photomultiplier tube pulses to the inputs for testing the entire instrument. Also, the sequential input to the A/D Converter is accessible on the front panel for monitoring on an oscilloscope.

The complete Sampling Digitizer is contained in a 24" x 24" x 78" cabinet (Fig. 1) and requires about 400 watts of 115V, 60 cps power. Most of the circuitry has been built on 4-1/2" x 5" or 4-1/2" x 6" printed-circuit cards. Both the signal and power leads connect via 22-pin printed-circuit connectors. Up to 29 printed-circuit cards plug into each 5-1/4" card file. The instrument has 12 card files, of which five are contained in two drawers. The inputs are located on the rear of the instrument, and all Monitor points and operating controls are on the front.

III. PARALLEL TO SERIAL CONVERTER

The Parallel to Serial Converter (see Fig. 3) transforms the 25 simultaneous signals at the Analog Inputs into 25 consecutive pulses, which can be analyzed by the Analog to Digital Converter. The inputs accept negative, fast pulses (~ 10 ns) either directly from photomultiplier tubes or from fast-gating circuits. Full scale (100) on the Sampling Digitizer corresponds to an integrated charge in the input pulse of 40 picocoulombs.

The fast input pulses (usually from fast gates) are stretched in a passive RLC shaper, which is a 1μs version of the 50 ns shaper previously

used by one of us.[3] It has a resistive, 125 ohm input impedance and produces a critically damped output pulse with a width at half maximum of 1μs. The shaper output is then delayed by 1μs in order to allow the trigger pulse from the preselection circuits to arrive as much as 0.7μs after the inputs. A grounded base stage is used to match the 125 ohm impedance required by the shaper to the 1000 ohm impedance of the delay line, thus providing a voltage gain of eight.

The output of the delay line is amplified in a feedback amplifier, which has a voltage gain of 250 and a rise time of 0.2μs. This amplifier consists of two transistors with feedback from the emitter of the output transistor to the base of the input transistor. The input impedance is 1000 ohms in order to terminate the delay line, and a third transistor is used to reduce the output impedance to about 25 ohms. The output of the amplifier drives the Analog Storage Card.

A simplified schematic of the Analog Storage Card is shown in Fig. 4. Transistors Q1, Q2, and Q3 form the linear Input Gate. The emitter of Q1 is connected to AC ground by a 100 ohm resistor, and thus the signal current appearing at the collector of Q1 is nearly the input voltage divided by 100 ohms. The collector current of Q2 is controlled by the 1000 ohm potentiometer labelled Pedestal Adjustment so that it just equals the DC collector current of Q1. This adjustment is relatively independent of temperature, since the drifts in the base-emitter voltages of Q1 and Q2 tend to cancel. Also, the +27V and -27V tend to drift together, which also tends to cancel in the pedestal drift. So long as the base of Q3 is clamped at -15V by the input gating pulse,

the signal current from the collector of Q1 will flow into the emitter of Q3 with no current passing through D1 onto the storage capacitor (C4-0.01μF). However, during the Read-in Phase when the input gating pulse is at zero, the signal current will flow through D1 and charge the storage capacitor (C4) by as much as 10V. The fact that the impedance of the source which charges the storage capacitor exceeds 100K during the Read-in Phase minimizes the instabilities and non-linearities introduced by the finite forward conductance of D1. During this time, Q7 normally holds the lower end of the storage capacitor at -12V. The impedance seen at its emitter is about 3 ohms, allowing C4 to be charged with its lower end effectively at AC ground. The input gating pulse will return to -15V in 5μs, leaving D1 cut off with C4 still charged. Thus, the circuit integrates its negative inputs during the 5μs that the Input Gate is open. The total charge gain from the Analog Input to the storage capacitor is 2500. Thus, to charge the capacitor by 10V requires 40pC at the input.

After the completion of the Read-in Phase, the Control initiates the Sampling Phase, during which the appropriate scanning gate causes Q6 to be pulsed into saturation. This causes Q7 to pull the lower end of C4 to ground, during which time the voltage on C4 appears at the input of the A/D Converter and is converted to two-digit decimal number. The Sampling Phase lasts 8ms when all 25 Analog Inputs are used.

At the end of the Sampling Phase, the voltage across C4 is set to zero by closing the mercury relay. During this Reset Phase, these relays are held closed for 3ms. A total of 8ms is allowed for them to close,

discharge the storage capacitors, and then open. The relay coil is driven by Q5 saturating when Q4 is cut off by a positive input pulse.

The accuracy of the Analog Storage is partly determined by the rate of discharge of the storage capacitor caused by the leakage currents and resistances of D1, D2, the diode in the mixer, and the mercury relay. At 10V reverse bias, the CD1438 diodes* have a leakage current of less than 1nA and a back resistance of 10,000 megohms. The Balance Adjustment controls the voltage on the anode of D2 so that its leakage tends to cancel the leakage of D1. Thus, the storage capacitor sees a total leakage current of less than 1nA, and the storage time constant is given by $0.01\mu F \times \frac{10,000}{4}$ megohms = 25 seconds.

During the Sampling Phase, the worst case for decay occurs when a 10V pulse must be stored for 8ms. In this case, the decay will be less than 4mV which is 0.04 per cent of full scale.

At the end of the Reset Phase, the leakage currents will cause the storage capacitor to charge at an initial rate of less than 0.1 V/s. Therefore, the Reset Phase is initiated whenever the Count Gate opens, so that the storage capacitors are reset no more than one second before the arrival of an accepted event.

The outputs of the 25 Analog Storage Cards are connected to the A/D Converter via a diode mixer and an amplifier. The diode mixer, using the low-leakage CD1438 diodes, follows the most positive of its inputs.

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* These diodes, purchased from Continental Devices Corporation of Los Angeles, California, are a selection of the 1N459 with a leakage current of less than 2nA at 100V and a forward conduction of at least 100 mA at 1V.

The output of the diode mixer is connected to an inverting DC amplifier with an input impedance greater than 30 megohms paralleled by 100pF. Three consecutive emitter followers with feedback from the emitter of the third to the collector of the first drive the base of a transistor with 25K in the emitter to ground. The output signal appears at the collector of this fourth transistor and is a current equal to the input voltage divided by 25K. The output pulse droops less than 0.1 per cent during the 300μs required by the analog to digital conversion.

Due to polarization effects in the dielectrics of the cards and connectors, the diodes of the 25 fold mixer were mounted on teflon stand-offs. The four-card files containing the Parallel to Serial Converter were constructed out of aluminum to prevent magnetic coupling of the Analog Inputs.

IV. PERFORMANCE

The Sampling Digitizer has been extensively tested with a precision mercury pulser and has been used with counter telescopes at the Caltech Synchrotron. The pulser tests show a linearity of better than $\pm$0.1 per cent of full scale. The interaction of any 24 inputs on the remaining one is less than one channel. Over several days with temperature variations of about 5^{o}C, the drifts have been less than 0.2 per cent of full scale. The instrument has required very little maintenance during several months of operation.

The entire system in which the instrument is presently being used consists of a 26-counter telescope array, electronic preselection,

Sampling Digitizer, analysis program, and the Burroughs 220. Particles are allowed to stop in a stack of 15 counters. The other counters have various functions, associated with triggering the system and measuring other aspects of the reaction being studied. A fast 4-fold coincidence-veto opens gates on the system, and amplitude discrimination is performed on 10 pulse heights.[3] If all criteria are satisfied, the Sampling Digitizer is triggered and records 18 Analog Inputs and 2 Digital Inputs.

A given run of data is broken up into units of arbitrary length on paper tape. Each unit is flagged by a single control word at its beginning. This word contains the run number, unit number, and numbers of Analog and Digital Inputs being used. A control word is also inserted to indicate the end of a roll of tape.

In an experiment now in progress (K^+ meson photoproduction), we are attempting particle identification by making a statistical fit to the rate of energy loss for each stopping particle satisfying the preselection requirements. An example from this experiment will serve to illustrate the behavior of the system.

The telescope and the preselection requirements were set to accept protons with energies between 250 and 340 MeV. Counters had previously been calibrated so that the Sampling Digitizer output for minimum ionizing particles was known to within 2 per cent. In Fig. 5 are plotted the light outputs of the first 14 counters in the system for a given proton event. The vertical bars represent expected statistical fluctuations in light output, and the horizontal bars indicate the counter thickness. This

proton had stopped in counter 15, and from the light output of this counter, its range and energy were established. Calculations of the likelihood of the particle being a stopping proton were made independently for the first 9 and the last 5 counters. The only selection on this event was that both of these likelihoods were near the maxima.

The whole motivation for recording information in a correlated form is evident in this example. Instead of collecting statistics in each counter for many particles, we can look at each particle in many counters. In this case we can say that the event is near the maximum of the proton likelihood distribution, and is very unlikely to be a K or π meson. Thus we can achieve a particle separation which would be difficult by other methods.

The Sampling Digitizer, together with the main core of the analysis program, is sufficiently general that no modification is required to use the system in a different experiment. The specific analysis procedure is very easily modified, a feature that has already proved useful. It is significant that in the present experiment, when some unforeseen difficulties appeared, analysis subsections of the program were re-written, but the existing data were not invalidated.

The chief limitation in the Sampling Digitizer as a general output system for complex high-energy physics experiments is the one event per second capability of the paper tape perforator. Therefore, the instrument has been modified so that its output can also be fed directly into a computer memory. Two rates are available in this mode of operation, one allowing 20 events per second and the other 60 events per second. The

slower rate has been successfully used with a data transmission link* to the Burroughs 220 computer. Plans are being made for the use of the higher rate with an IBM 7090 computer. Paper tape remains as an optional output medium.

There are two classes of experiments for which the paper tape recording rate is not a serious limitation. One is the pure counter experiment in which sufficient accuracy is obtained with a few thousand counts. Examples of this are polarization experiments and strange particle photoproduction. Counting rates are made reasonable by increasing angular and energy resolutions. The limitation to approximately 150 bits of information per event does not seriously limit the complexity of such a counter array. Another class of experiments involves recording counter and coincidence circuit outputs associated with photographs of visual detectors such as spark chambers. The Sampling Digitizer is easily capable of assimilating the counter outputs of any experiment being done in this laboratory, and will permit greater freedom in planning more complicated future experiments.

ACKNOWLEDGMENTS

It would be nearly impossible to specifically acknowledge all the persons connected with the production of this instrument. The aid of Professor Matthew Sands in supplying over-all supervision of the project

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* The design and construction of this data transmission link and the modifications of the Burroughs 220 computer were performed by the Caltech Computing Center.

is gratefully appreciated. The cooperation of Ransom Research in solving the various technical and administrative difficulties involved was invaluable. Specifically, Mr. David Ransom, Sr., General Manager of Ransom Research and Vice-President of Wyle Laboratories, was most tolerant of the difficulties arising from a joint development project between an industrial concern and a university. Mr. Norman Grannis, of Ransom Research, was responsible for the design and operation of the Temporary Storage, Data Multiplexer, and the associated parts of the Control. Mr. Arpad Barna, then of Ransom Systems and now with the University of Chicago, supervised the construction of the Parallel to Serial Converter and the Analog to Digital Converter and designed the parts of the Control essential to their operation.

APPENDIX. ANALOG TO DIGITAL CONVERTER

The Analog to Digital Converter generates 25 consecutive pairs of binary-coded decimal digits, each pair of which is a number proportional to the output voltage of the Parallel to Serial Converter corresponding to one Analog Input.

A simplified block diagram of the A/D Converter is shown in Fig. 6. Each of the two Trial Voltage Generators contains four flip-flops connected to a ladder adder. The ladder adder generates an analog voltage depending on the state of each flip-flop and sums the four voltages thus formed. When a flip-flop is in the "0" state, its corresponding analog voltage is zero. When the first flip-flop is in the "1" state, its corresponding voltage has a relative value of 1, the second flip-flop produces a relative voltage of 2, the third 4, and the fourth 8. The absolute value of the voltage is determined by the voltage reference. If all four flip-flops can be in either the "0" or "1" state without any restrictions, then all possible four bit binary numbers can be decoded into analog voltages corresponding to any integral value between 0 and 15. For binary-coded decimal output, a lockout circuit insures that 9 is the highest voltage generated. The Tens and Units Trial Voltage Generators are summed, with the tens given a weight of 10 while the units have a weight of 1. Thus, for binary-coded decimal output, an analog voltage corresponding to any channel between 0 and 99 can be generated by the proper combination of the eight flip-flops of the Trial Voltage Generators.

The summed output of the Trial Voltage Generators is subtracted from the input voltage, and the difference is compared with zero by a DC amplifier. The output of this amplifier is used to control the flip-flops of the Trial Voltage Generators.

The timing sequence during the analog to digital conversion is as follows: Initially all flip-flops in the Trial Voltage Generators are set to the "0" state. At the end of the first clock pulse, the flip-flop with a relative analog voltage of 80 is set to the "1" state. If 80 exceeds the input voltage, then the flip-flop is reset to "0" on command of the DC amplifier. If the input exceeds 80, then the flip-flop is left in its "1" state. The cycle continues in order of decreasing relative analog voltage until all eight flip-flops of the Trial Voltage Generators have been correctly set. Thus, a two-decimal-digit binary-coded decimal number is generated whose relative analog voltage is smaller than the input voltage by the least possible amount. This number is then transferred to the Temporary Storage, and the Trial Voltage Generators are reset in preparation for the next input.

The principal advantages of this system are twofold. Firstly, the output is a binary-coded decimal number which is very easy to store without the need for shift registers or other counting circuitry. Secondly, the time required to perform a conversion is independent of the input amplitude. Also, this technique appears more efficient than a basically analog technique, such as a linear rundown of a capacitor. The principal disadvantage of this system is that extreme accuracy is required in the digital to analog converter. This becomes particularly crucial in the

channels whose least significant digit is 9. For these channels, the upper boundary is determined by the Tens Trial Voltage Generator, while the lower boundary is determined by the Unit Trial Voltage Generator. If these are not accurately matched, the width of this channel will differ considerably from the others. Thus, although only 100 channels are resolved, the A/D Converter has to be a 0.1 per cent instrument in order to keep the channel widths uniform to 10 per cent. Since the Sampling Digitizer is intended for applications where absolute values of correlated pulse heights are measured, the uniformity of the channel widths is not particularly important. Therefore, in contrast to most pulse height analyzers, this type of A/D Converter was found suitable.

FIGURE CAPTIONS

FIGURE 1: Photographs of the Sampling Digitizer.

FIGURE 2: Functional Block Diagram.

FIGURE 3: Block Diagram - Parallel to Serial Converter.

FIGURE 4: Simplified Schematic-Analog Storage Card.

FIGURE 5: A Single 300-MeV Proton Stopping in Counter Telescope.

FIGURE 6: Simplified Block Diagram - Analog to Digital Converter.

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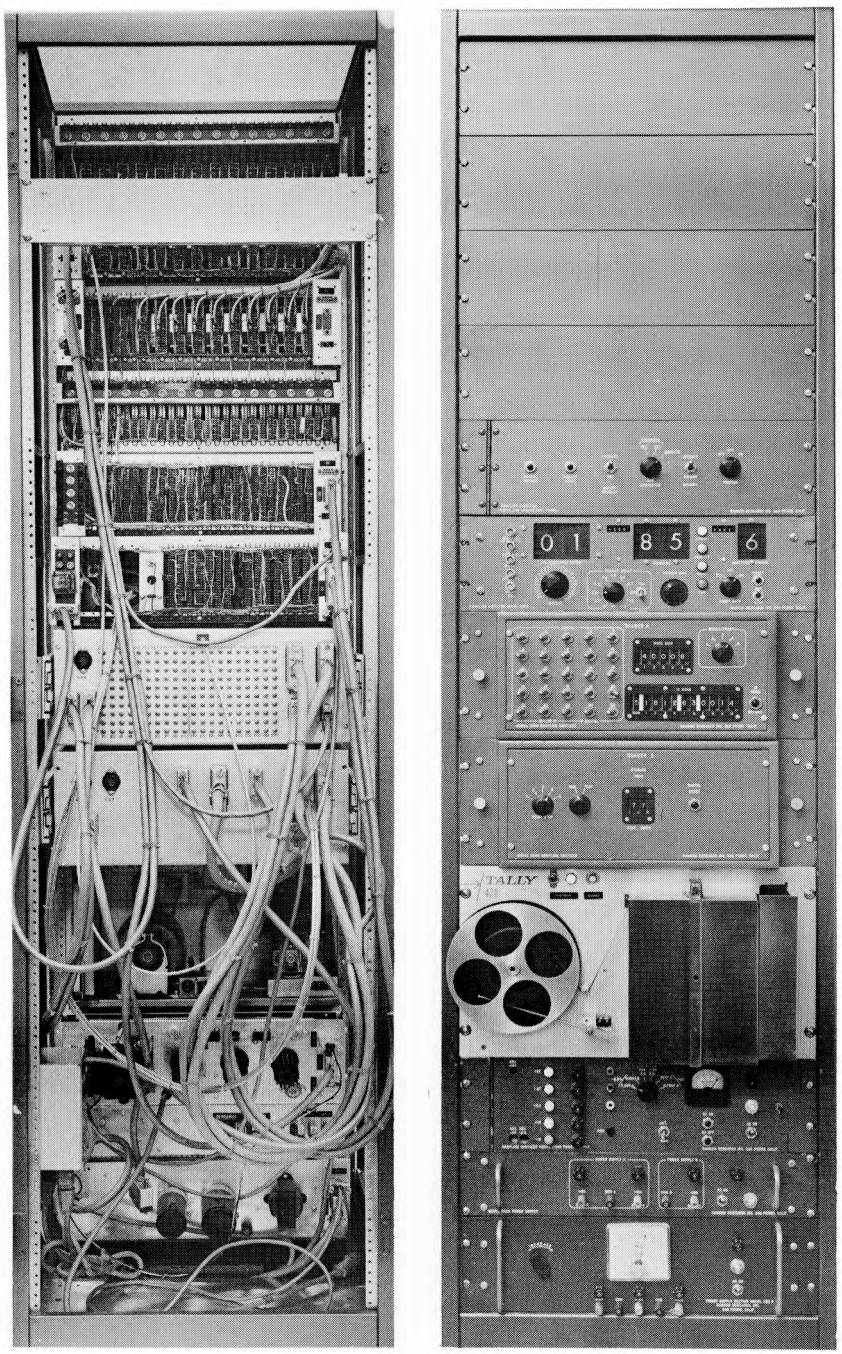
2. C. C. Rockwood and M. G. Strauss, Rev. Sci. Instr. 32, 1211 (1961).

3. A. Barna, J. H. Marshall, and M. Sands, Nuclear Instruments and Methods 12, 43 (1961).



BACK FRONT

FIGURE 1: Photographs of the Sampling Digitizer

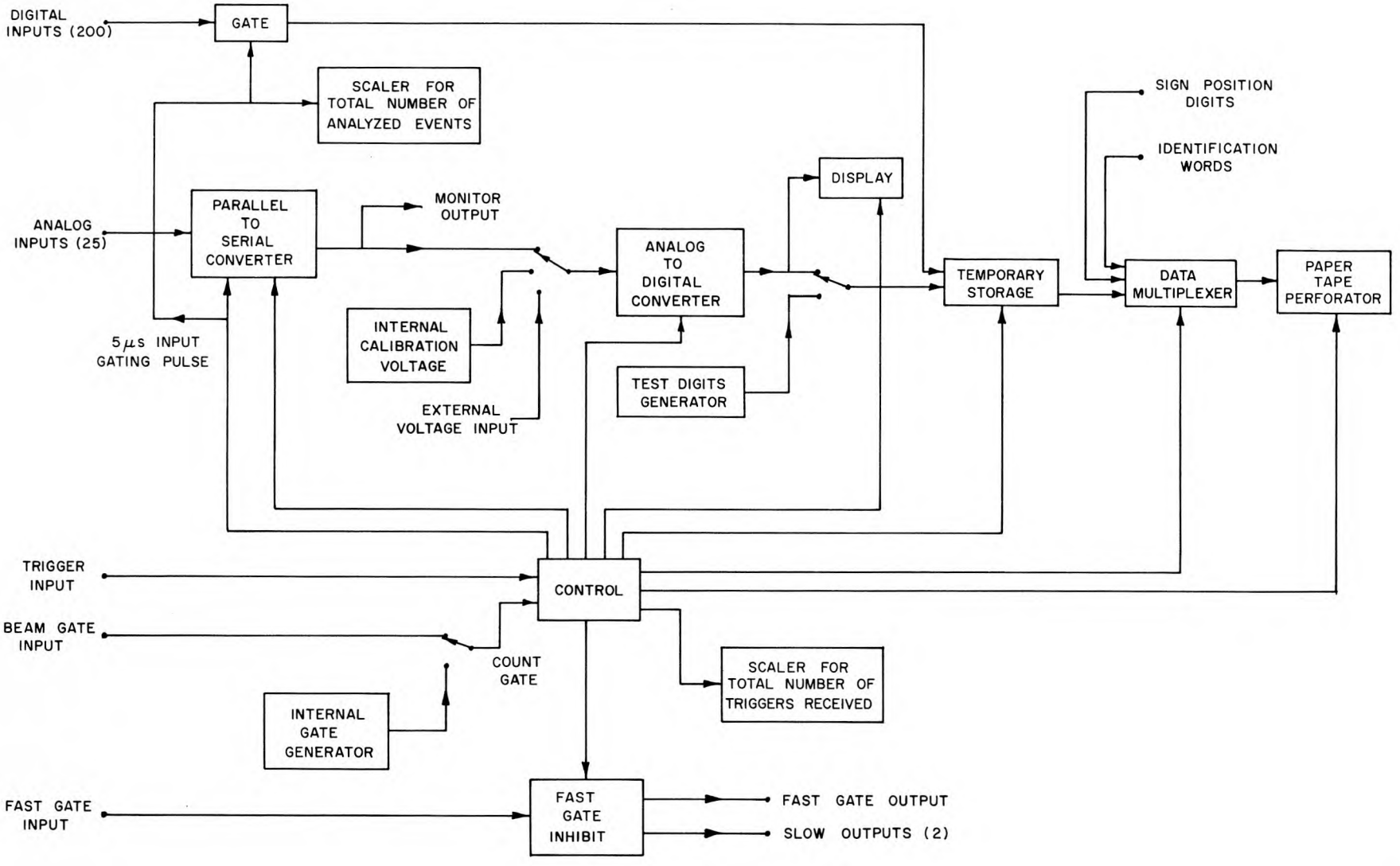


FIGURE 2: Functional Block Diagram

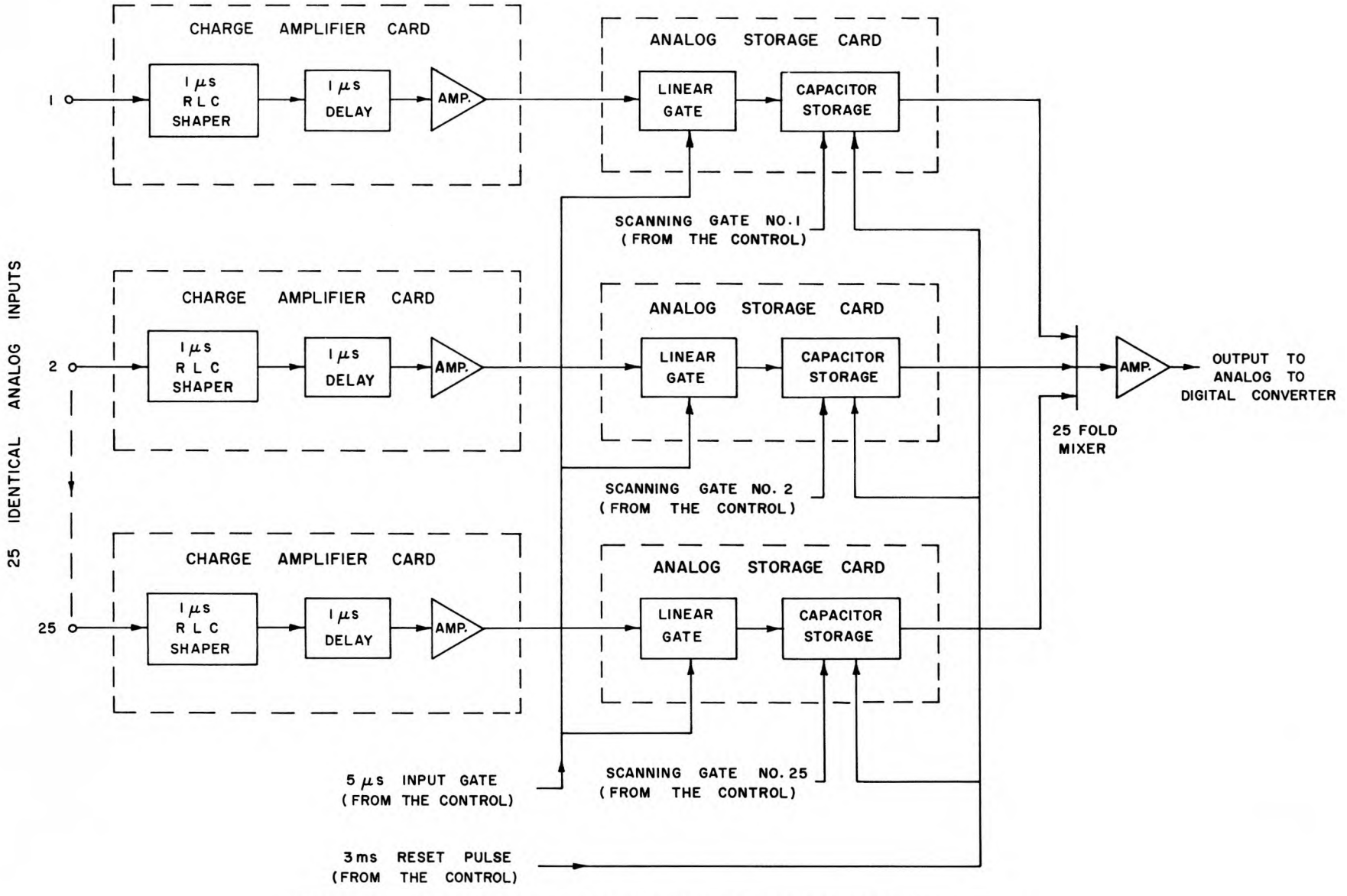


FIGURE 3: Block Diagram of the Parallel to Serial Converter

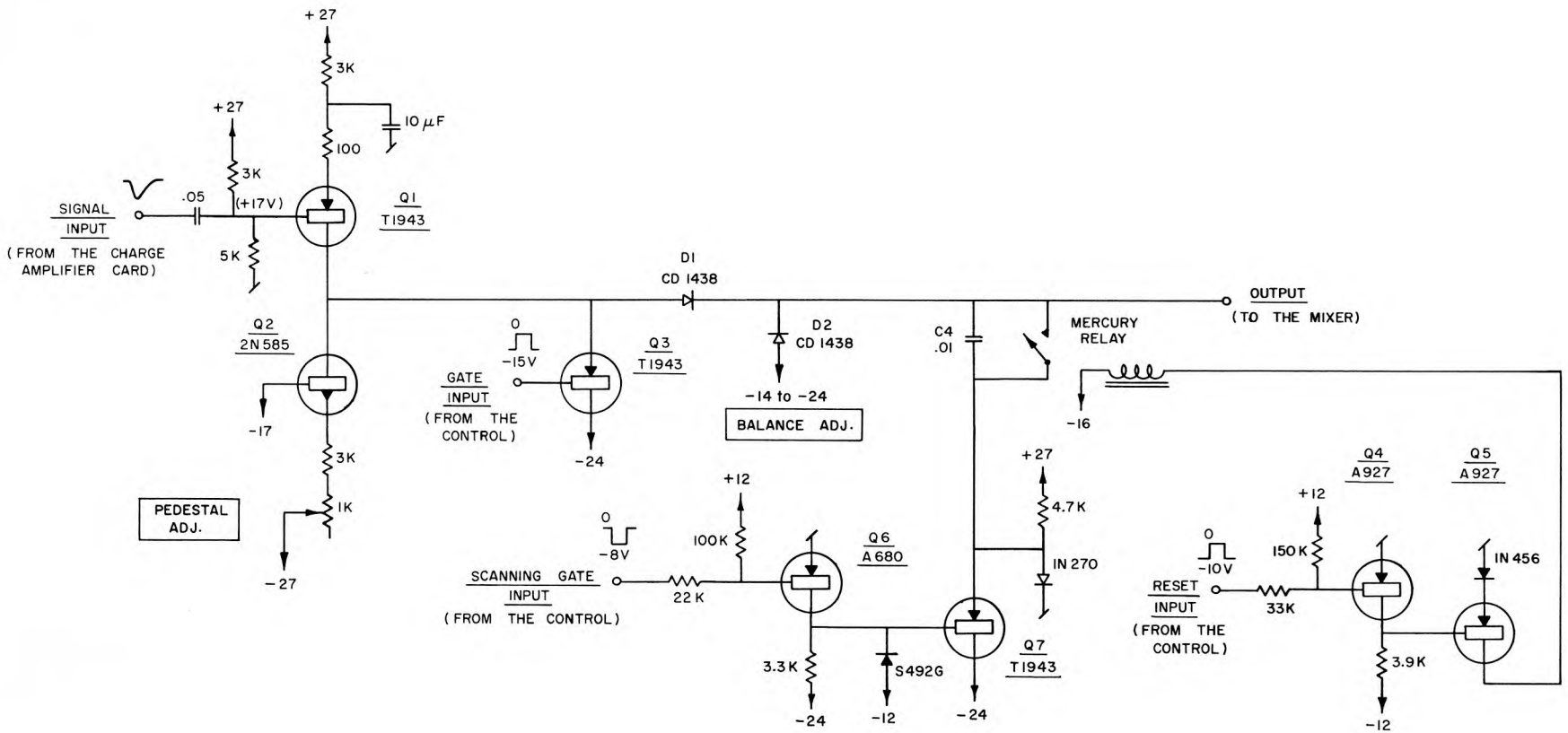


FIGURE 4: Simplified Schematic of the Analog Storage Card

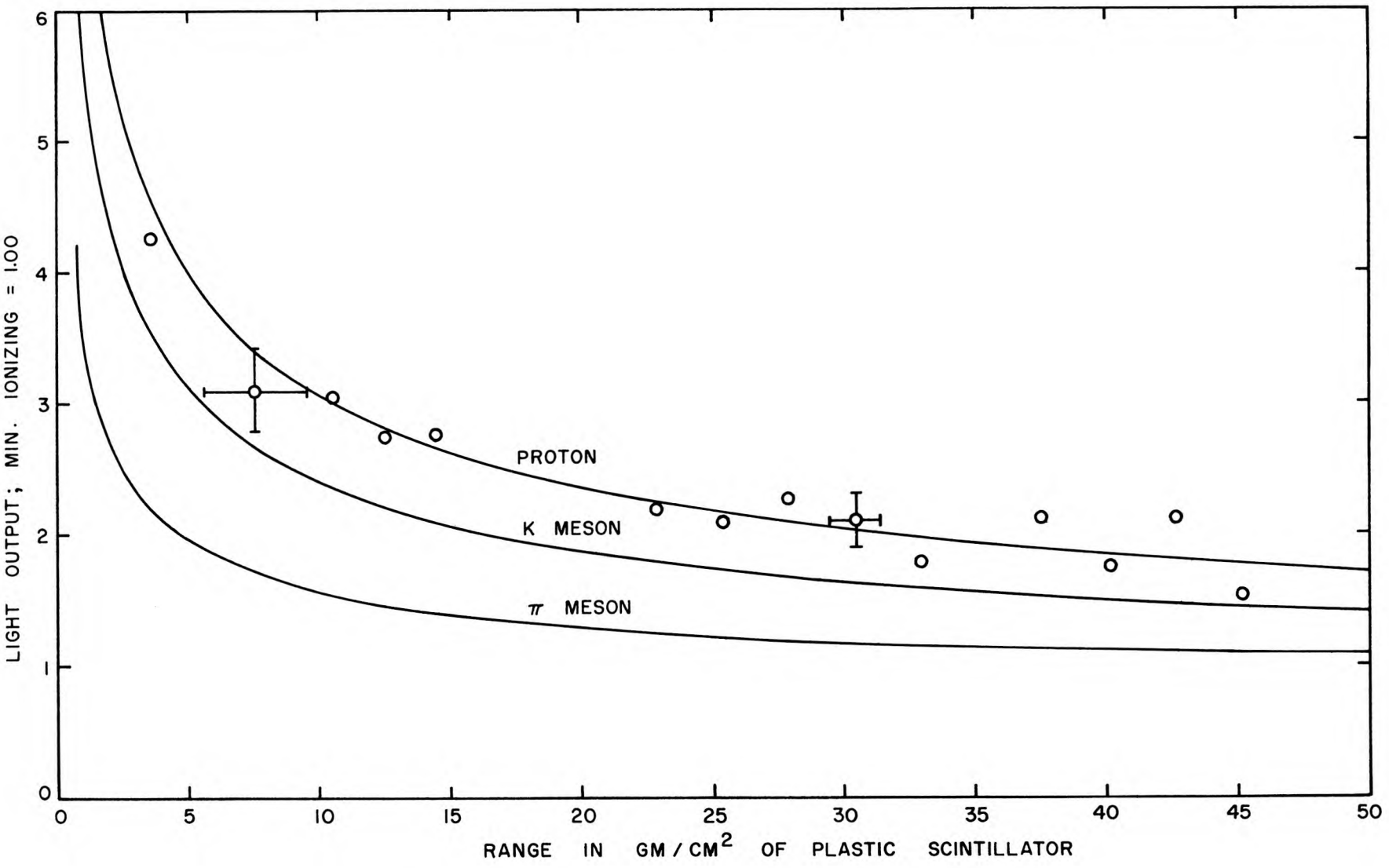


FIGURE 5: A Single 300-Mev Proton Stopping in the Counter Telescope

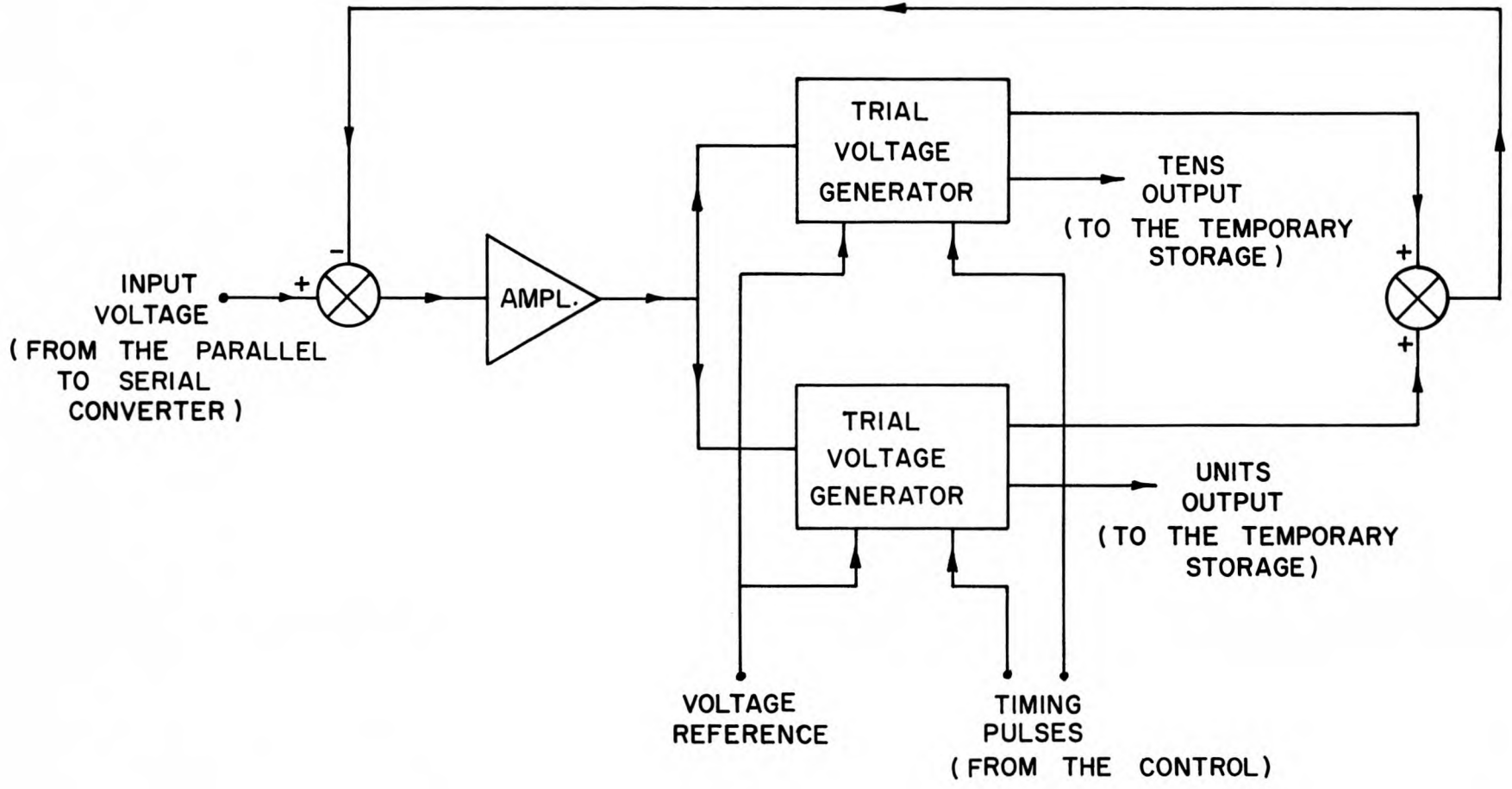


FIGURE 6: Block Diagram of the Analog to Digital Converter